MICRO-37

Microarchitecture Micro 37 Proceedings

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Adaptable Embedded Systems Antonio Carlos Schneider Beck,Carlos Arthur Lang Lisbôa,Luigi Carro,2012-11-27 As embedded systems become more complex designers face a number of challenges at different levels they need to boost performance while keeping energy consumption as low as possible they need to reuse existent software code and at the same time they need to take advantage of the extra logic available in the chip represented by multiple processors working together This book describes several strategies to achieve such different and interrelated goals by the use of adaptability Coverage includes reconfigurable systems dynamic optimization techniques such as binary translation and trace reuse new memory architectures including homogeneous and heterogeneous multiprocessor systems communication issues and NOCs fault tolerance against fabrication defects and soft errors and finally how one can combine several of these techniques together to achieve higher levels of performance and adaptability The discussion also includes how to employ specialized software to improve this new adaptive system and how this new kind of software must be designed and programmed **Proceedings** ,2005 Designing Embedded Processors Jörg Henkel,Sri Parameswaran,2007-07-27 As we embrace the world of personal portable and perplexingly complex digital systems it has befallen upon the bewildered designer to take advantage of the available transistors to produce a system which is small fast cheap and correct yet possesses increased functionality Increasingly these systems have to consume little energy Designers are increasingly turning towards small processors which are low power and customize these processors both in software and hardware to achieve their objectives of a low power system which is verified and has short design turnaround times Designing Embedded Processors examines the many ways in which processor based systems are designed to allow low power devices It looks at processor design methods memory optimization dynamic voltage scaling methods compiler methods and multi processor methods Each section has an introductory chapter to give a breadth view and have a few specialist chapters in the area to give a deeper perspective The book provides a good starting point to engineers in the area and to research students embarking upon the exciting area of embedded systems and architectures Computer Architecture Performance Evaluation Methods Lieven Eeckhout,2022-05-31 Performance evaluation is at the foundation of computer architecture research and development Contemporary microprocessors are so complex that architects cannot design systems based on intuition and simple models only Adequate performance evaluation methods are absolutely crucial to steer the research and development process in the right direction However rigorous performance evaluation is non trivial as there are multiple aspects to performance evaluation such as picking workloads selecting an appropriate modeling or simulation approach running the model and interpreting the results using meaningful metrics Each of these aspects is equally important and a performance evaluation method that lacks rigor in any of these crucial aspects may lead to inaccurate performance data and may drive research and development in a wrong direction The goal of this book is to present an overview of the current state of the art in computer

architecture performance evaluation with a special emphasis on methods for exploring processor architectures The book focuses on fundamental concepts and ideas for obtaining accurate performance data The book covers various topics in performance evaluation ranging from performance metrics to workload selection to various modeling approaches including mechanistic and empirical modeling And because simulation is by far the most prevalent modeling technique more than half the book s content is devoted to simulation The book provides an overview of the simulation techniques in the computer designer s toolbox followed by various simulation acceleration techniques including sampled simulation statistical simulation parallel simulation and hardware accelerated simulation Table of Contents Introduction Performance Metrics Workload Design Analytical Performance Modeling Simulation Sampled Simulation Statistical Simulation Parallel Simulation and Hardware Acceleration Concluding Remarks **Multicore Processors and Systems** Stephen W. Keckler,Kunle Olukotun,H. Peter Hofstee,2009-08-29 Multicore Processors and Systems provides a comprehensive overview of emerging multicore processors and systems It covers technology trends affecting multicores multicore architecture innovations multicore software innovations and case studies of state of the art commercial multicore systems A cross cutting theme of the book is the challenges associated with scaling up multicore systems to hundreds of cores The book provides an overview of significant developments in the architectures for multicore processors and systems It includes chapters on fundamental requirements for multicore systems including processing memory systems and interconnect It also includes several case studies on commercial multicore systems that have recently been developed and deployed across multiple application domains The architecture chapters focus on innovative multicore execution models as well as infrastructure for multicores including memory systems and on chip interconnections The case studies examine multicore implementations across different application domains including general purpose server media broadband network processing and signal processing Multicore Processors and Systems is the first book that focuses solely on multicore processors and systems and in particular on the unique technology implications architectures and implementations The book has contributing authors that are from both the academic and industrial communities Networks-on-Chip Sheng Ma,Libo Huang,Mingche Lai,Wei Shi,2014-12-04 Networks on Chip From Implementations to Programming Paradigms provides a thorough and bottom up exploration of the whole NoC design space in a coherent and uniform fashion from low level router buffer and topology implementations to routing and flow control schemes to co optimizations of NoC and high level programming paradigms This textbook is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture and Networks on Chip It is also intended for practitioners in the industry in the area of microprocessor design especially the many core processor design with a network on chip Graduates can learn many practical and theoretical lessons from this course and also can be motivated to delve further into the ideas and designs proposed in this book Industrial engineers can refer to this book to make practical tradeoffs as well Graduates and engineers

who focus on off chip network design can also refer to this book to achieve deadlock free routing algorithm designs Provides thorough and insightful exploration of NoC design space Description from low level logic implementations to co optimizations of high level program paradigms and NoCs The coherent and uniform format offers readers a clear quick and efficient exploration of NoC design space Covers many novel and exciting research ideas which encourage researchers to further delve into these topics Presents both engineering and theoretical contributions The detailed description of the router buffer and topology implementations comparisons and analysis are of high engineering value **Transactions on High-Performance Embedded Architectures and Compilers IV** Per Stenström,2011-11-22 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This 4th issue contains 21 papers carefully reviewed and selected out of numerous submissions and is divided in four sections The first section contains five regular papers The second section consists of the top four papers from the 4th International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2009 held in Paphos Cyprus in January 2009 The third section contains a set of six papers providing a snap shot from the Workshop on Software and Hardware Challenges of Manycore Platforms SHCMP 2008 held in Beijing China in June 2008 The fourth section consists of six papers from the 8th IEEE International Symposium on Systems Architectures Modeling and Simulation SAMOS VIII 2008 held in Samos Greece in July 2008 **Processor Microarchitecture** Antonio González,Fernando Latorre,Grigorios Magklis,2010-12-30 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an

advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture It is also intended for practitioners in the industry in the area of microprocessor design The book assumes that the reader is familiar with the main concepts regarding pipelining out of order execution cache memories and virtual memory Table of Contents Introduction Caches The Instruction Fetch Unit Decode Allocation The Issue Stage Execute The Commit Stage References Author Biographies **Dynamic Binary Modification** Kim Hazelwood,2022-05-31 Dynamic binary modification tools form a software layer between a running application and the underlying operating system providing the powerful opportunity to inspect and potentially modify every user level guest application instruction that executes Toolkits built upon this technology have enabled computer architects to build powerful simulators and emulators for design space exploration compiler writers to analyze and debug the code generated by their compilers software developers to fully explore the features bottlenecks and performance of their software and even end users to extend the functionality of proprietary software running on their computers Several dynamic binary modification systems are freely available today that place this power into the hands of the end user While these systems are quite complex internally they mask that complexity with an easy to learn API that allows a typical user to ramp up fairly quickly and build any of a number of powerful tools Meanwhile these tools are robust enough to form the foundation for software products in use today This book serves as a primer for researchers interested in dynamic binary modification systems their internal design structure and the wide range of tools that can be built leveraging these systems The hands on examples presented throughout form a solid foundation for designing and constructing more complex tools with an appreciation for the techniques necessary to make those tools robust and efficient Meanwhile the reader will get an appreciation for the internal design of the engines themselves Table of Contents Dynamic Binary Modification Overview Using a Dynamic Binary Modifier Program Analysis and Debugging Active Program Modification Architectural Exploration Advanced System Internals Historical Perspectives Summary and Observations **Cyber Physical Systems. Design, Modeling, and Evaluation** Roger Chamberlain,Walid Taha,Martin Törngren,2019-04-12 This book constitutes the proceedings of the 7th International Workshop on Design Modeling and Evaluation of Cyber Physical Systems CyPhy2017 held in conjunction with ESWeek 2017 in Seoul South Korea in October 2017 The 10 papers presented together with 1 extended and 1 invited abstracts in this volume were carefully reviewed and selected from 16 submissions The conference presents a wide range of domains including robotics smart homes vehicles and buildings medical implants and future generation sensor networks **Network-on-Chip Architectures** Chrysostomos Nicopoulos,Vijaykrishnan Narayanan,Chita R. Das,2009-09-18 2 The Cell Processor from Sony Toshiba and IBM STI 3 and the Sun UltraSPARC T1 formerly codenamed Niagara 4 signal the growing popularity of such systems Furthermore Intel s very recently announced 80 core TeraFLOP chip 5 exemplifies the irreversible march toward many core systems with tens or even hundreds of processing elements 1 2 The Dawn of the Communication Centric Revolution The multi core thrust has ushered

the gradual displacement of the computati centric design model by a more communication centric approach 6 The large sophisticated monolithic modules are giving way to several smaller simpler p cessing elements working in tandem This trend has led to a surge in the popularity of multi core systems which typically manifest themselves in two distinct incarnations heterogeneous Multi Processor Systems on Chip MPSoC and homogeneous Chip Multi Processors CMP The SoC philosophy revolves around the technique of Platform Based Design PBD 7 which advocates the reuse of Intellectual Property IP cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations The appeal of such a modular approach lies in the substantially reduced Time To Market TTM incubation period which is a direct outcome of lower circuit complexity and reduced design effort The whole system can now be viewed as a diverse collection of pre existing IP components integrated on a single die *Heterogeneous Computing* Mohamed Zahran,2019-05-29 If you look around you will find that all computer systems from your portable devices to the strongest supercomputers are heterogeneous in nature The most obvious heterogeneity is the existence of computing nodes of different capabilities e g multicore GPUs FPGAs But there are also other heterogeneity factors that exist in computing systems like the memory system components interconnection etc The main reason for these different types of heterogeneity is to have good performance with power efficiency Heterogeneous computing results in both challenges and opportunities This book discusses both It shows that we need to deal with these challenges at all levels of the computing stack from algorithms all the way to process technology We discuss the topic of heterogeneous computing from different angles hardware challenges current hardware state of the art software issues how to make the best use of the current heterogeneous systems and what lies ahead The aim of this book is to introduce the big picture of heterogeneous computing Whether you are a hardware designer or a software developer you need to know how the pieces of the puzzle fit together The main goal is to bring researchers and engineers to the forefront of the research frontier in the new era that started a few years ago and is expected to continue for decades We believe that academics researchers practitioners and students will benefit from this book and will be prepared to tackle the big wave of heterogeneous computing that is here to stay **Dark Silicon and Future On-chip Systems** ,2018-07-26 Dark Silicon and the Future of On chip Systems Volume 110 the latest release in the Advances in Computers series published since 1960 presents detailed coverage of innovations in computer hardware software theory design and applications with this release focusing on an Introduction to dark silicon and future processors a Revisiting of processor allocation and application mapping in future CMPs in the dark silicon era Multi objectivism in the dark silicon age Dark silicon aware resource management for many core systems Dynamic power management for dark silicon multi core processors Topology specialization for networks on chip in the dark silicon era and Emerging SRAM based FPGA architectures Provides in depth surveys and tutorials on new computer technology Covers well known authors and researchers in the field Presents extensive bibliographies with most chapters Includes volumes that are devoted to single

themes or subfields of computer science with this release focusing on Dark Silicon and Future On chip Systems **Rugged Embedded Systems** Augusto Vega,Pradip Bose,Alper Buyuktosunoglu,2016-12-02 Rugged Embedded Systems Computing in Harsh Environments describes how to design reliable embedded systems for harsh environments including architectural approaches cross stack hardware software techniques and emerging challenges and opportunities A harsh environment presents inherent characteristics such as extreme temperature and radiation levels very low power and energy budgets strict fault tolerance and security constraints etc that challenge the computer system in its design and operation To guarantee proper execution correct safe and low power in such scenarios this contributed work discusses multiple layers that involve firmware operating systems and applications as well as power management units and communication interfaces This book also incorporates use cases in the domains of unmanned vehicles advanced cars and micro aerial robots and space exploration as examples of computing designs for harsh environments Provides a deep understanding of embedded systems for harsh environments by experts involved in state of the art autonomous vehicle related projects Covers the most important challenges fault tolerance power efficiency and cost effectiveness faced when developing rugged embedded systems Includes case studies exploring embedded computing for autonomous vehicle systems advanced cars and micro aerial robots and space exploration **Performance Analysis and Tuning for General Purpose Graphics Processing Units (GPGPU)** Hyesoon Kim,Richard Vuduc,Sara Baghsorkhi,2012 General purpose graphics processing units GPGPU have emerged as an important class of shared memory parallel processing architectures with widespread deployment in every computer class from high end supercomputers to embedded mobile platforms Relative to more traditional multicore systems of today GPGPUs have distinctly higher degrees of hardware multithreading hundreds of hardware thread contexts vs tens a return to wide vector units several tens vs 1 10 memory architectures that deliver higher peak memory bandwidth hundreds of gigabytes per second vs tens and smaller caches scratchpad memories less than 1 megabyte vs 1 10 megabytes In this book we provide a high level overview of current GPGPU architectures and programming models We review the principles that are used in previous shared memory parallel platforms focusing on recent results in both the theory and practice of parallel algorithms and suggest a connection to GPGPU platforms We aim to provide hints to architects about understanding algorithm aspect to GPGPU We also provide detailed performance analysis and guide optimizations from high level algorithms to low level instruction level optimizations As a case study we use n body particle simulations known as the fast multipole method FMM as an example We also briefly survey the state of the art in GPU performance analysis tools and techniques **Electronic Business: Concepts, Methodologies, Tools, and Applications** Lee, In,2008-12-31 Enhances libraries worldwide through top research compilations from over 250 international authors in the field of e business

Dynamic Reconfigurable Architectures and Transparent Optimization Techniques Antonio Carlos Schneider Beck Fl.,Luigi Carro,2010-03-10 Dynamic Reconfigurable Architectures and Transparent Optimization Techniques presents a

detailed study on new techniques to cope with the aforementioned limitations First characteristics of reconfigurable systems are discussed in details and a large number of case studies is shown Then a detailed analysis of several benchmarks demonstrates that such architectures need to attack a diverse range of applications with very different behaviours besides supporting code compatibility This requires the use of dynamic optimization techniques such as Binary Translation and Trace reuse Finally works that combine both reconfigurable systems and dynamic techniques are discussed and a quantitative analysis of one them the DIM architecture is presented **Compiler Construction** Rajiv Gupta,2010-03-10 This book constitutes the refereed proceedings of the 19th International Conference on Compiler Construction CC 2010 held in Paphos Cyprus in March 2010 as part of ETAPS 2010 the Joint European Conferences on Theory and Practice of Software Following a thorough review process 16 research papers were selected from 56 submissions Topics covered include optimization techniques program transformations program analysis register allocation and high performance systems **Circuits and Systems Advances in Near Threshold Computing** Sanghamitra Roy,2021-05-11 Modern society is witnessing a sea change in ubiquitous computing in which people have embraced computing systems as an indispensable part of day to day existence Computation storage and communication abilities of smartphones for example have undergone monumental changes over the past decade However global emphasis on creating and sustaining green environments is leading to a rapid and ongoing proliferation of edge computing systems and applications As a broad spectrum of healthcare home and transport applications shift to the edge of the network near threshold computing NTC is emerging as one of the promising low power computing platforms An NTC device sets its supply voltage close to its threshold voltage dramatically reducing the energy consumption Despite showing substantial promise in terms of energy efficiency NTC is yet to see widescale commercial adoption This is because circuits and systems operating with NTC suffer from several problems including increased sensitivity to process variation reliability problems performance degradation and security vulnerabilities to name a few To realize its potential we need designs techniques and solutions to overcome these challenges associated with NTC circuits and systems The readers of this book will be able to familiarize themselves with recent advances in electronics systems focusing on near threshold computing FPGAs and Parallel Architectures for Aerospace Applications Fernanda Kastensmidt,Paolo Rech,2015-12-07 This book introduces the concepts of soft errors in FPGAs as well as the motivation for using commercial off the shelf COTS FPGAs in mission critical and remote applications such as aerospace The authors describe the effects of radiation in FPGAs present a large set of soft error mitigation techniques that can be applied in these circuits as well as methods for qualifying these circuits under radiation Coverage includes radiation effects in FPGAs fault tolerant techniques for FPGAs use of COTS FPGAs in aerospace applications experimental data of FPGAs under radiation FPGA embedded processors under radiation and fault injection in FPGAs Since dedicated parallel processing architectures such as GPUs have become more desirable in aerospace applications due to high computational power GPU analysis under radiation is also

discussed

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